REMARKS

Claims 1-18, all the claims pending in the application, are amended herein. The Office Action indicates that claims 4, 6, 10 and 16 contain allowable subject matter. Claims 5, 8 and 14 stand rejected upon informalities. Claims 1-3, 5, 7-9, 11-15 and 17-18 stand rejected on prior art grounds. Moreover, the specification is objected to because of informalities. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Objections to the Specification

The specification is objected to because of informalities. As such, Applicants have amended the specification to remove the offending language in accordance with the suggestions in the Office Action. Moreover, Applicants have further reviewed the specification and have amended it to correct minor grammatical errors. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections.

II. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 5, 8 and 14 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Accordingly, Applicants have amended claims 5, 8, and 14 to more fully point out and distinctly claim the subject matter including clarifying the claimed language and providing proper antecedent basis for the claimed language.

III. The Prior Art Rejections

Claims 1-3, 5, 7-9, 11-15 and 17-18 stand rejected under 35 U.S.C. §102(e) as being anticipated by Yamaki (U.S. Patent 6,446,213 - the Office Action refers to the Yamaki reference as U.S. Patent 6,447,213, which appears to be a misprint). Applicants respectfully traverse these rejections based on the following discussion.

Yamaki teaches before a register provided exclusively for an Advanced Configuration and Power Interface (ACPI) is set, a System Management Interrupt (SMI) is issued to a Central Processing Unit (CPU). A System Management-Basic Input Output System (SM-BIOS) performs the power management of a computer system. Values representing a wakeup factor of the system and a power management event are set in the register, and an Operating System Directed Power Management System (OSPM) is informed of a Power Management Event (PME). When the values are set in the register, an SMI is issued to the CPU, and the SM-BIOS performs the power management of the computer system.

However, the amended claimed invention includes features, which are patentably distinguishable from the prior art reference of record. Specifically, independent claims 1, 7, and 13 recite, in part, "...wherein said process event comprises an event for switching said computer from an energy-saving mode to a normal mode, and said additional process event comprises an event for switching said computer from said normal mode to the energy-saving mode after said process event is output." These features are simply not taught or suggested in Yamaki.

There are several key differences between Yamaki and the claimed invention. First, Yamaki teaches a method of establishing an ACPI-compliant system with non-ACPI-compliant hardware and software using a SMI (System Management Interrupt) handler. Conversely, the

claimed invention teaches a system and method of handling a user's request to/upon the system and a technique of switching the computer from a sleeping state to a normal mode and back again to a sleeping/standby state.

Conversely, Yamaki teaches the setting of triggers for waking up the system from a sleeping/suspend state. Specifically, ACPI defines the hardware for enabling/disabling the hardware event, which allows the system to wake up from the sleeping/standby state. The "hooking" of the operating system involves programming the hardware into the sleeping state. Moreover, ACPI defines the hardware to control the system power state. In this regard Yamaki teaches that the SMI handler can hook and control the hardware instead of the operating system. The ACPI includes management of the power state (power supply from AC or battery, or the remaining battery status), or the thermal condition information, and Yamaki teaches that this management can be implemented using the SMI handler.

Conversely, the claimed invention provides that every hardware and software complies with the ACPI specification. In one example of implementing the claimed invention, the "eject button" is pressed while the computer is attached to a docking station and while the computer is in the sleeping/standby state. However, the ACPI specification does not define this type of event. Therefore, the original equipment manufacturer (OEM) maps this event to some event defined in the ACPI specification. In this case, the user simply desires to eject the computer. However, the user does not want to wake the system up and leave it in a normal (wake up) state. As such, in order to detach the computer, the operating system performs some house-keeping. Therefore, the hardware/BIOS wakes the system up, allows the operating system to run, requests the operating system to handle the detaching event, and then returns the computer to the sleeping/standby state

(energy saving mode). However, in Yamaki, the ACPI does not define how to request the operating system to perform another event in this regard. Rather, the claimed invention teaches a unique and novel way to do this. Accordingly, in the claimed invention, the BIOS requests the operating system to put the computer system in the sleeping state again after completion of the process event.

Additionally, column 6, lines 13-63 of Yamaki indicate how the switching from the normal state to the sleeping state occurs:

> PWRBTN_STS is a register which is set when the power supply switch of the computer system is pushed. When both PWRBTN_EN (not shown) and PWRBTN_STS are set while the computer system remains in the normal state, a system control interrupt (SCI) is issued. The SCI is a system interrupt the hardware uses to inform the OSPM 120 of a power management event (hereinafter referred to as "PME (Power Management Event)." When the power supply switch is depressed while the computer system remains in the sleep state or the soft-off state, a wakeup event is generated in the embedded controller (EC) 18, no matter whether the resister PWRBTN_EN has been set. Usually, the PWRBTN_STS bit is set by the hardware only, if the PWRBTN_STS register is of ACPI specification. The PWRBTN_STS register is reset only when "1" is written at the PWRBTN_STS bit by means of the software.
>
> In the computer system of the invention, the EC 18 issues an SMI before the PWRBTN_STS register is set. In response to the SMI, the SM-BIOS sets the bit, issuing an system control interrupt (SCI) to the OSPM 120.
>
> RTC-STS is a register which is set when the real time clock (RTC) 15 asserts an alarm, i.e., an IRQ signal. If RTC_EN (not shown) is set and if the RT_STS bit is set, the hardware will inform the OSPM 120 of the power management event (PME). Usually, the RTC_STS bit is set by the hardware only, if the RTC_STS register is of ACPI specification. The RTC_STS register is reset only when "1" is written at the RTC_STS bit by means of the software. While the computer system stays in the sleep state, the RTC_STB bit must be set before a control is returned to the OSPM 120 if the real time clock (RTC) 15 has caused a wakeup event.

> In the computer system of the invention, the EC 18 issues an SMI before the RTC_STS register is set. In response to the SMI, the SM-BIOS sets the bit, issuing an SCI to the OSPM 120.
>
> WAK_STS is a register which is set when a [sic] wakeup event happens as the power supply switch or the real time clock (RTC) 15 is operated while the computer system remains in the sleep state. When the WAK_STS bit is set, the computer system is set into the normal state. According to the ACPI specification, the WAK_STS bit is usually set by the hardware only. The WAK_STS register is reset only when "1" is written at the RTC_STS bit by means of the software.
>
> In the computer system of this invention, the EC 18 issues an SMI before the WAK_STS register is set. In response to the SMI, the SM-BIOS sets the bit, issuing an SCI to the OSPM 120. WAK_STS is a register which is set when an wakeup event happens as the power supply switch or the real time clock (RTC) 15 is operated while the computer system remains in the sleep state. When the WAK_STS bit is set, the computer system is set into the normal state. According to the ACPI specification, the WAK_STS bit is usually set by the hardware only. The WAK_STS register is reset only when "1" is written at the RTC_STS bit by means of the software.
>
> In the computer system of this invention, the EC 18 issues an SMI before the WAK_STS register is set. In response to the SMI, the SM-BIOS sets the bit, issuing an SCI to the OSPM 120.

The above-language in Yamaki tends to teach away from the claimed invention. Specifically, Yamaki indicates that "when the power supply switch is depressed while the computer system remains in the sleep state or the soft-off state, a wakeup event is generated in the embedded controller." This indicates that the power supply switch triggers the wakeup event. The claimed invention is not limited to this triggering mechanism. Rather an attach/detach event may trigger the wakeup event. Furthermore, Yamaki indicates that "WAK_STS is a register which is set when a [sic] wakeup event happens as the power supply switch or the real time clock

(RTC) 15 is operated while the computer system remains in the sleep state." This further indicates that the wakeup event is time-dependent, that is when the RTC is operated. Again, the claimed invention does not directed to this.

In view of the foregoing, Applicants respectfully submit that Yamaki does not teach or suggest the features defined by amended independent claims 1, 7, and 13 and as such, claims 1, 7, and 13 are patentable over Yamaki. Further, dependent claims 2-6, 8-12, and 14-18 are similarly patentable over Yamaki, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

IV. Formal Matters and Conclusion

With respect to the objections/rejections to the claims and specification, the claims and specification have been amended to overcome these objections/rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-18, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the

Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Assignee's Deposit Account Number 50-0510.

Respectfully submitted,

Dated: 6/28/04

Mohammad S. Rahman
Reg. No. 43,029
McGinn & Gibb, P.L.L.C.
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (301) 261-8625
Fax: (301) 261-8825
Customer Number: 29154